REMARKS

Claims 18-29 are presently pending. Claims 18-28 were rejected. Claim 29 is added. Reconsideration and continued examination are respectfully requested.

The specification and drawings are objected to for failing to comply with 37 CFR 1.84(p)(5). Assignee has made amendments to the specification and drawings and respectfully submits that the foregoing objections are now overcome.

Claim 18 was rejected under 35 U.S.C. § 101 for statutory double patenting with respect to claim 9 of U.S. Patent U.S. Patent 7,284,072.

MPEP 804.II.A states:

> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. "Same invention" means identical subject matter. *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).
>
> A reliable test for double patenting under 35 U.S.C. 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970). Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist. For example, the invention defined by a claim reciting a compound having a "halogen" substituent is not identical to or substantively

> the same as a claim reciting the same compound except having a "chlorine" substituent in place of the halogen because "halogen" is broader than "chlorine." On the other hand, claims may be differently worded and still define the same invention. Thus, a claim reciting a widget having a length of "36 inches" defines the same invention as a claim reciting the same widget having a length of "3 feet."
>
> If it is determined that the same invention is being claimed twice, 35 U.S.C. 101 precludes the grant of the second patent regardless of the presence or absence of a terminal disclaimer. *Id.*

Assignee respectfully traverses the rejection under 35 U.S.C. § 101 because embodiments exist that there are embodiment(s) of the invention that falls within the scope of one claim, but not the other. The chart below shows claim 18 of the present application and claim 9 of the '072 application in their entirety.

18. A direct memory access controller, said direct memory access controller comprising:	9. A system for providing a plurality of sequential data words, said method comprising:
a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words; and	a state logic machine for receiving a command to provide the plurality of sequential data words, wherein the plurality of sequential data words comprises a first data word and a last data word, and one or more data words between the first data word and the last data word, and wherein the plurality of sequential data words occupy an amount of memory in a first memory;
a memory controller for	a memory controller for

fetching a first portion of the range and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command.	fetching a sequential portion of the sequential data words, said sequential portion comprising a first intermediate word, the last word, and one or more data words between the intermediate word and the last word;
	a local buffer for identically storing the sequential portion, comprising less than the amount of memory occupied by the plurality of sequential data words in the first memory; and
	a port for transmitting at least a portion of the last data word and transmitting at least a portion of the intermediate data words after transmitting at least the portion of the last data word.

It can be seen, for example (and not as an exhaustive list), that a device that does not include "a local buffer … comprising *less than the amount of memory occupied by the plurality of sequential data words* in the first memory" could infringe claim 18, but not claim 9 of the '072 patent.

Accordingly, Assignee respectfully traverses the rejection to claim 18 for double patenting under 35 U.S.C. § 101. It is noted that Assignee has filed a terminal disclaimer with respect to the '072 patent, thereby obviating any obviousness double patenting rejection.

Claims 18 and 24 were rejected under 35 U.S.C. §

102(a) as anticipated by Lee. The Final Office Action (FOA) indicated that Lee teaches "a state logic machine (fig. 4, state machine 404; and fig. 12, FSM 1206) for receiving a single command (fig. 5, control command 501; and fig. 6, command 601) to provide a specific range (col. 11, lines 15-19, address range of external memory to be accessed) of a plurality of sequential data words (col. 4, lines 24-29, accessed memory blocks has plurality of sequential data words)".

Assignee respectfully traverses the rejection because Lee does not disclose "a state logic machine for receiving a single command". Although Examiner has indicated that Lee teaches "a state logic machine (fig. 4, state machine 404; and fig. 12, FSM 1206)", the "state machine 404" and "FSM 1206" do not receive commands. Rather, the "co-processor interface 402 interprets the coprocessor command data generated from RISC processor 207". It is noted that Examiner reads "single command" on Figure 5, control command 501, and Figure 6, Command 601. However, Fig. 5 and Fig 6 are views illustrating the coprocessor command sets used at the coprocessor interface 402." Thus, Lee does not disclose "a state logic machine for receiving a *single* command" (claim 18) or "receiving a single command" (claim 24).

Additionally, Assignee argued in the response to the previous office action that commands "501 and 601 do not include the capability to specify a range of data words. See Col. 10, Line 59 - Col. 11, Line 36. Accordingly, Lee does not teach "a single command to provide a *specified … range* of a plurality of sequential data words" (claim 18).

Examiner now indicates that Lee "discloses the command 601 contains fields such as CRd to select external memory

as first range, internal DEC memory as second range, and local memory as third possible range". Examiner also makes citation to col. 11, lines 15-19.

Assignee respectfully traverses the rejection. It is first noted that command 501 is "used for reading or writing the register of each block included in VDEC 203". "CRn 505 represents the upper 4 bits of the register address to be used", "CRm represents the lower 4 bits of the register address to be used". The foregoing is not "a specified … range of a plurality of sequential data words" (claim 18). Turning to command 601, CRd merely identifies which memory is used. It appears from the Office Action that Examiner's position is that identification of a memory to be used is the specification of a range of addresses, the range being the first data word to the last data word of the identified memory.

However, even if, arguendo, identification of a memory is held to be specification of a range being the first data word to the last data word of the identified memory, Assignee respectfully submits that identification of a memory is not "a single command to provide" all of the words from the first data word of the identified memory to the last word of the identified memory. Moreover, Assignee has amended claim 18 to recite "specified *selectable* range". The foregoing would not be "selectable". Additionally, the identification of a memory clearly would not teach "wherein the specified selectable range of the plurality of sequential data words *is less than a memory storing the plurality of sequential data words*" as claimed in claim 30.

Additionally, Assignee also traverses because the command 601 is not received by the VDEC 203, Lee teaches

that VDEC 203 "should inform to RISC processor 207 by using a command 601, and then RISC processor 207 can access data through main bus 211." Col. 11, Lines 15-19. Thus, instead of VDEC 203 "receiving" the command 601, VDEC actually issues command 601 for the RISC processor 207.

Examiner has also indicated that Lee teaches "a memory controller (fig. 11, buffer controller 1113) for fetching a first portion (fig. 11, portion of VLD input buffer 1112) of the range and a second portion (fig. 11, portion of VLD input buffer 1112) of the range after fetching the first portion". Office Action at 8.

Assignee respectfully traverses the rejection because it is noted that "the range" takes antecedent basis from "a state logic machine for receiving a single command to provide a specified selectable range of a plurality of sequential data words". However, even if arguendo, the specified range is "col. 11, lines 15-19, address range of external memory to be accessed", it is noted that the portions of the VLD input buffer 1112 are not portions of "the range" specified by the single command. Accordingly, Assignee also traverses the rejection to claim 18 for this additional reason.

Accordingly, Assignee respectfully requests withdrawal of the rejection to claims 18 and 24 and dependent claims 19-23, 25-28, and allowance of claim 29.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance.

The office action makes various other statements

regarding the invention that are now moot and will not be addressed. Assignee reserves the right to respond to these statements in the future, should the need arise.

The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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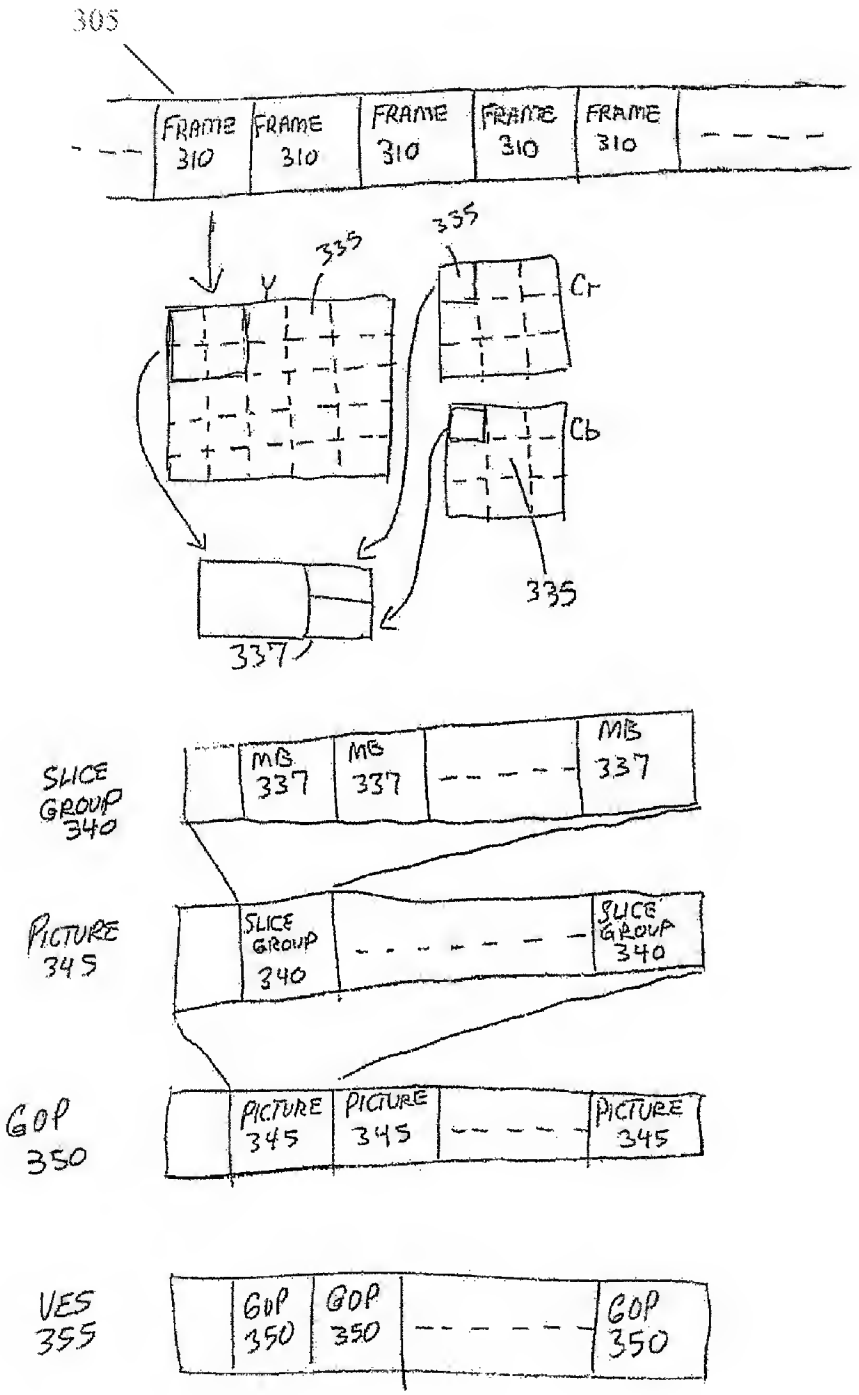
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FIG 1

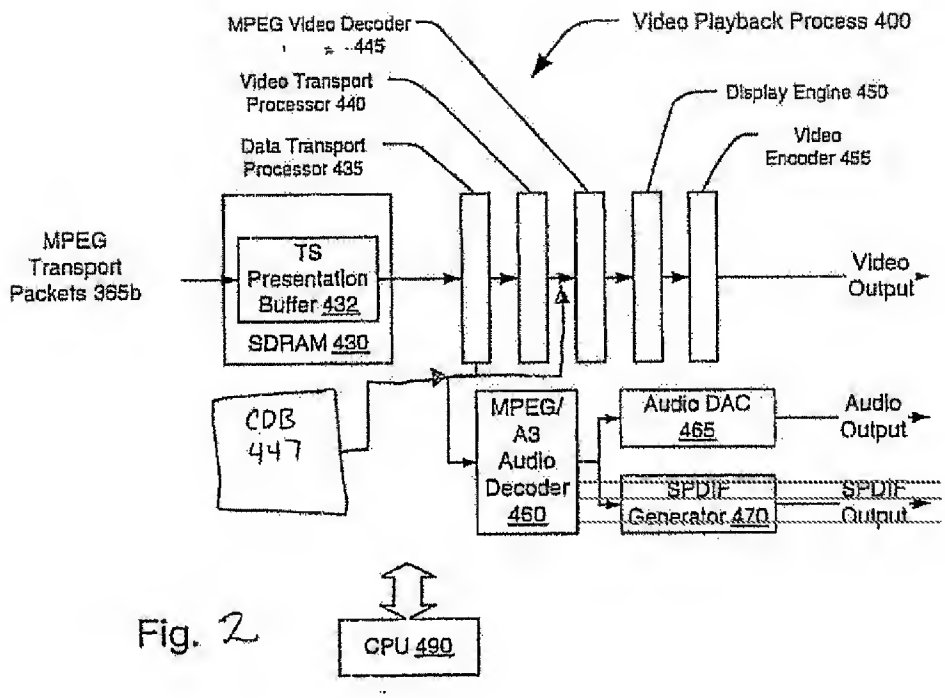
MPEG Video Decoder 445
Video Playback Process 400
Video Transport Processor 440
Display Engine 450
Data Transport Processor 435
Video Encoder 455
MPEG Transport Packets 365b
TS Presentation Buffer 432
SDRAM 430
Video Output
CDB 447
MPEG/ A3 Audio Decoder 460
Audio DAC 465
Audio Output
SPDIF Generator 470
SPDIF Output
CPU 490

Fig. 2

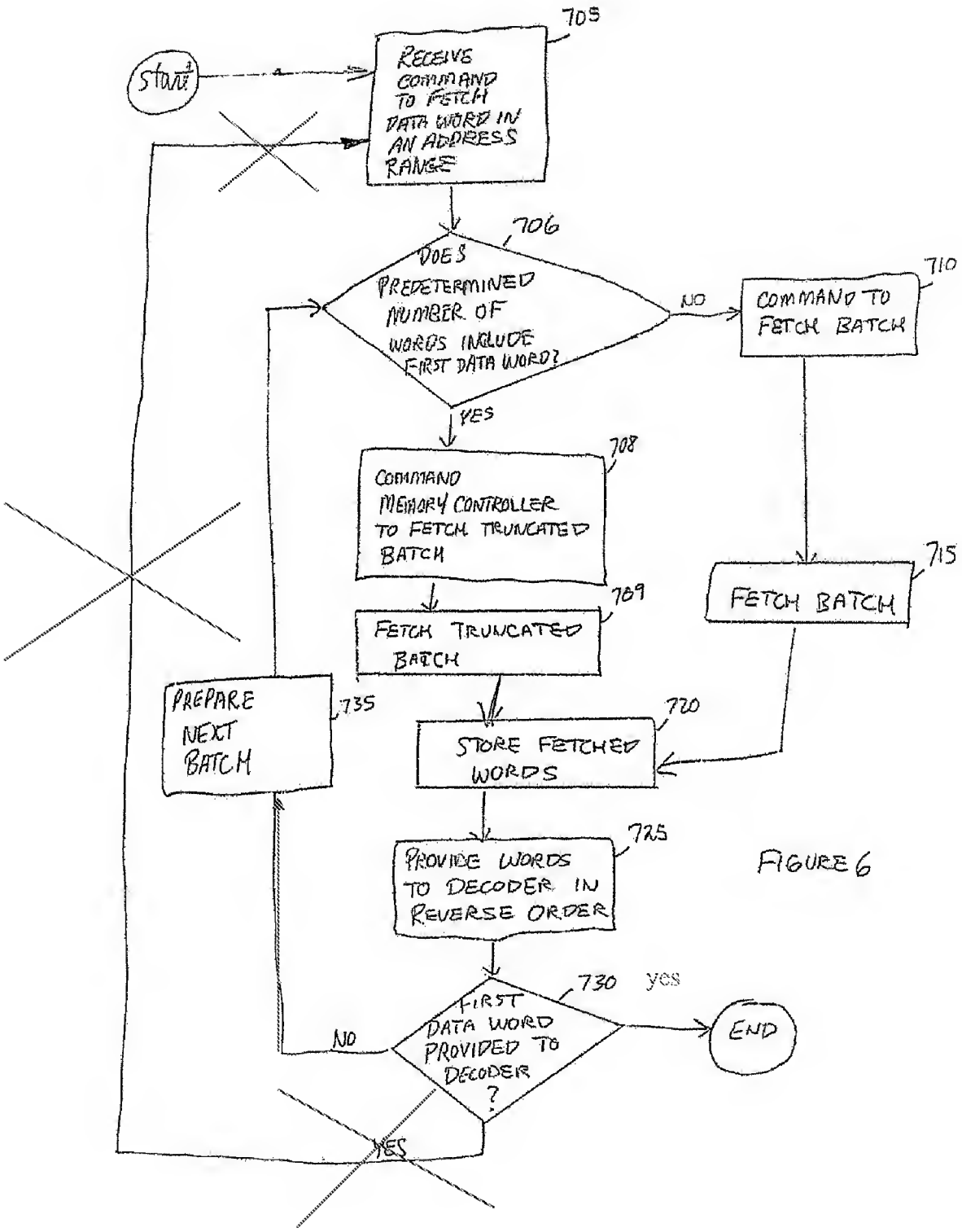
START
705
RECEIVE COMMAND TO FETCH DATA WORD IN AN ADDRESS RANGE
706
DOES PREDETERMINED NUMBER OF WORDS INCLUDE FIRST DATA WORD?
NO
YES
710
COMMAND TO FETCH BATCH
708
COMMAND MEMORY CONTROLLER TO FETCH TRUNCATED BATCH
709
FETCH TRUNCATED BATCH
715
FETCH BATCH
735
PREPARE NEXT BATCH
720
STORE FETCHED WORDS
725
PROVIDE WORDS TO DECODER IN REVERSE ORDER
730
FIRST DATA WORD PROVIDED TO DECODER ?
yes
NO
YES
END

FIGURE 6